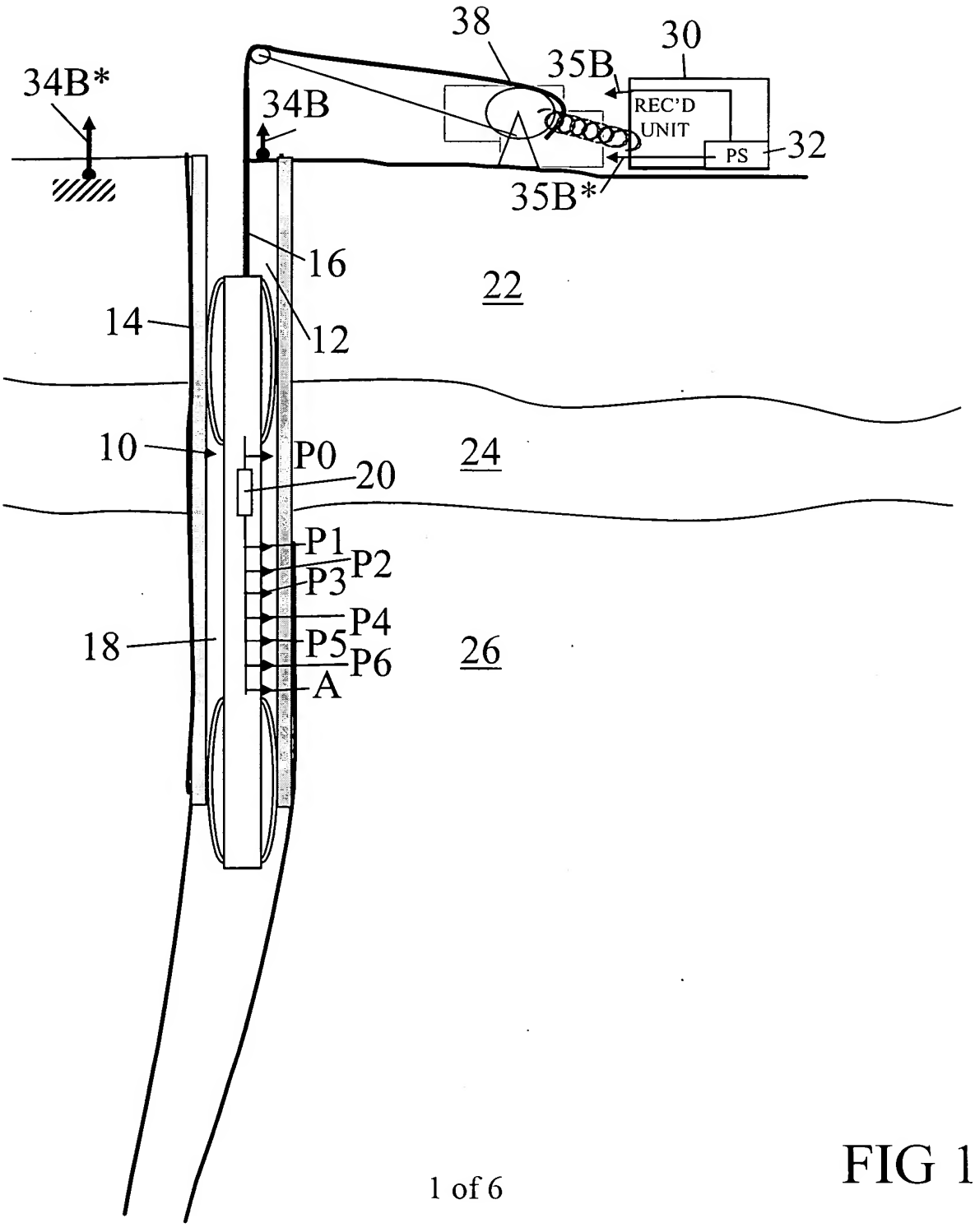
38
30
35B
34B*
34B
REC'D
UNIT
PS
32
35B*
16
22
14
12
10
P0
24
20
P1
P2
P3
P4
18
P5
P6
26
A

FIG 1

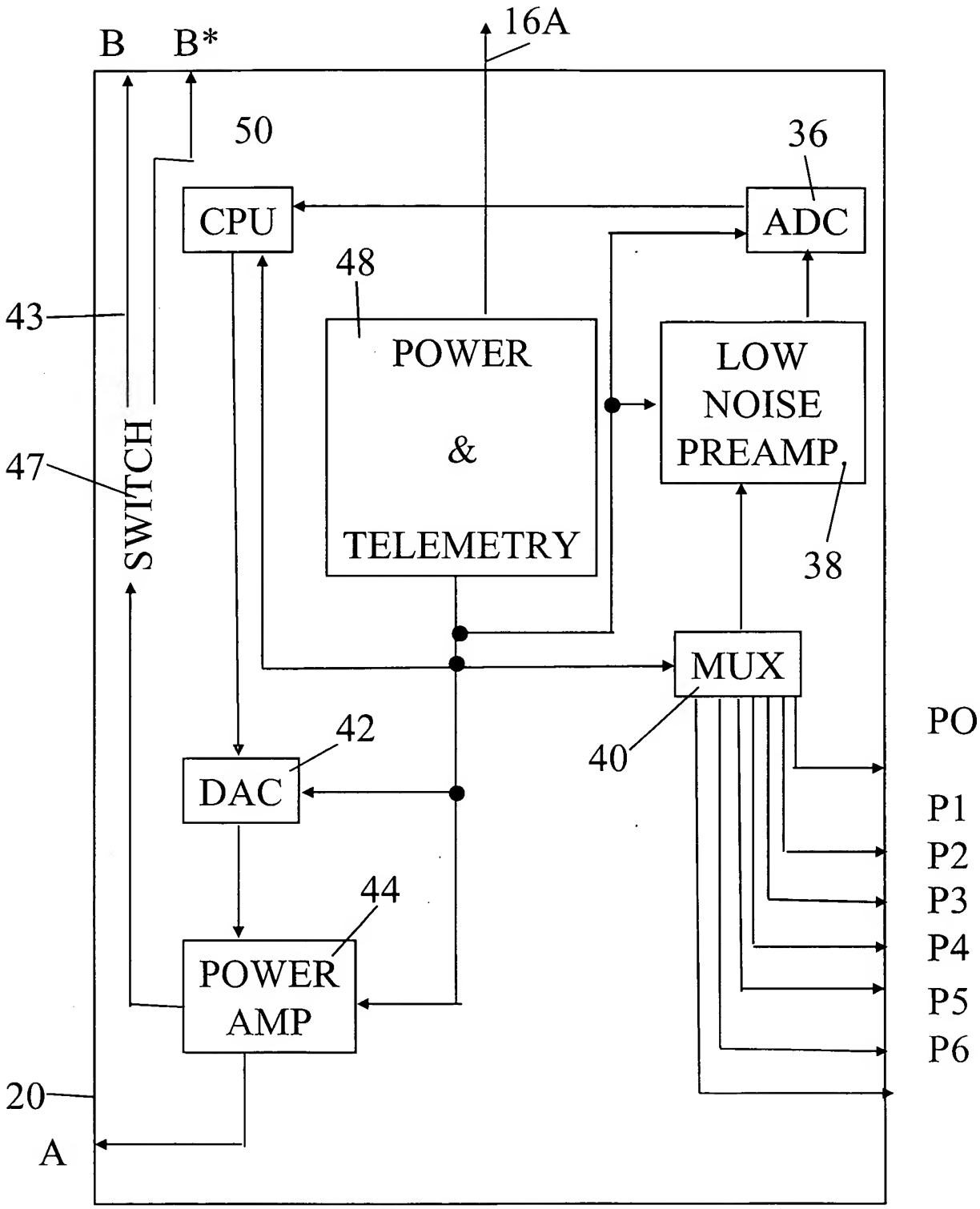
B
B*
16A
50
36
CPU
ADC
48
43
POWER
&
TELEMETRY
LOW
NOISE
PREAMP
47
SWITCH
38
MUX
PO
42
40
DAC
P1
P2
P3
44
P4
POWER
AMP
P5
P6
20
A

FIG 2

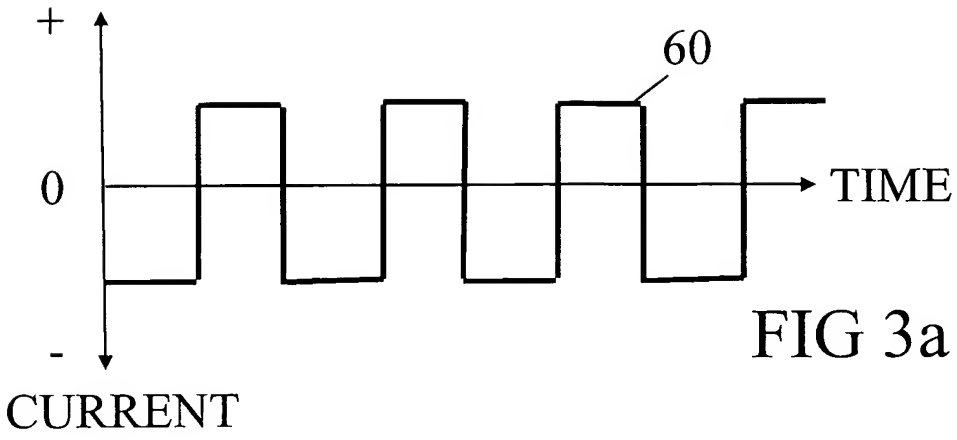

FIG 3a

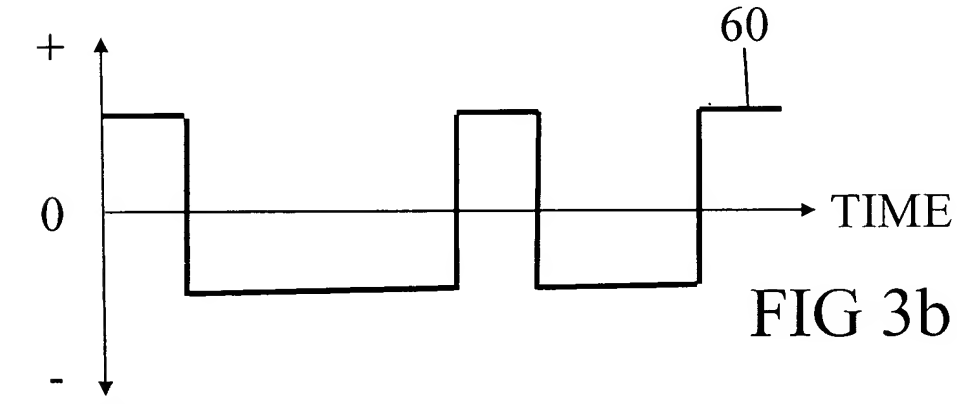

FIG 3b

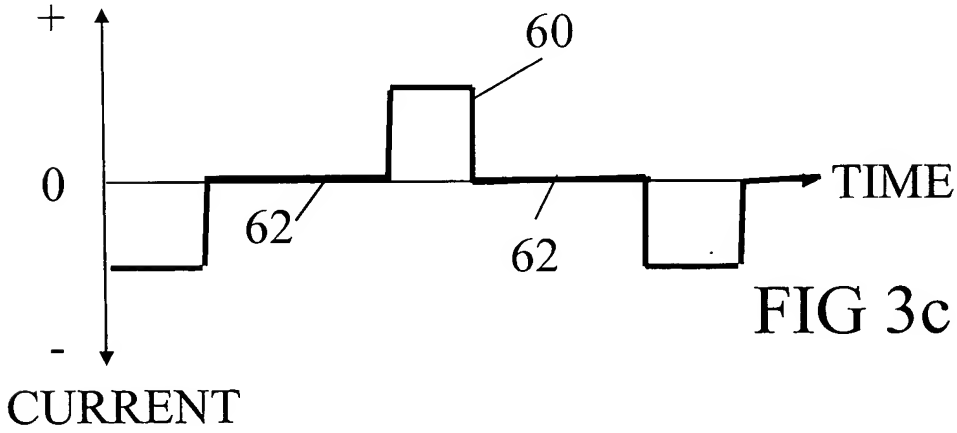

FIG 3c

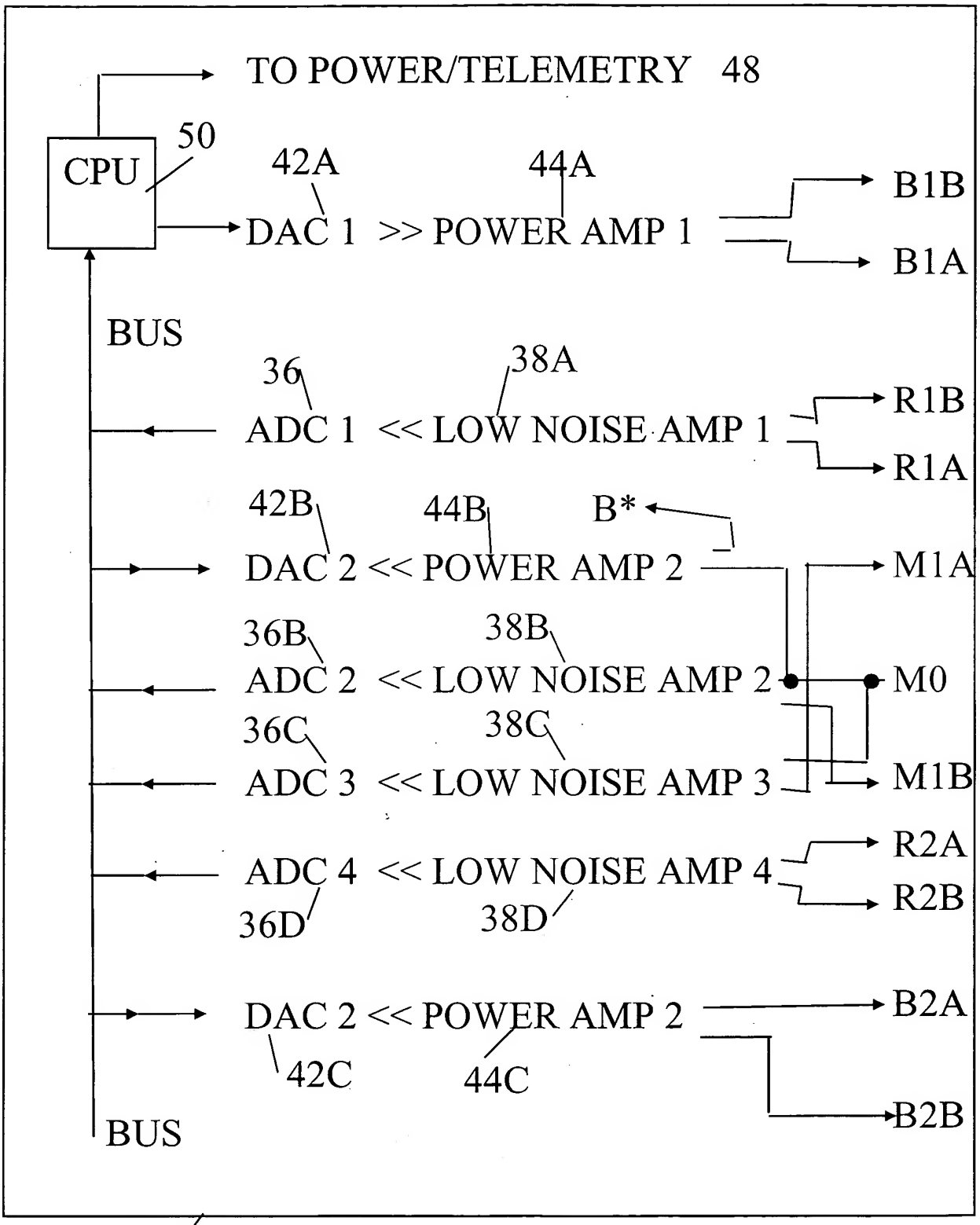
TO POWER/TELEMETRY 48
CPU
50
42A
44A
DAC 1 >> POWER AMP 1
B1B
B1A
BUS
36
38A
ADC 1 << LOW NOISE AMP 1
R1B
R1A
42B
44B
B*
DAC 2 << POWER AMP 2
M1A
36B
38B
ADC 2 << LOW NOISE AMP 2
M0
36C
38C
ADC 3 << LOW NOISE AMP 3
M1B
ADC 4 << LOW NOISE AMP 4
R2A
R2B
36D
38D
DAC 2 << POWER AMP 2
B2A
42C
44C
B2B
BUS
20A

FIG 4

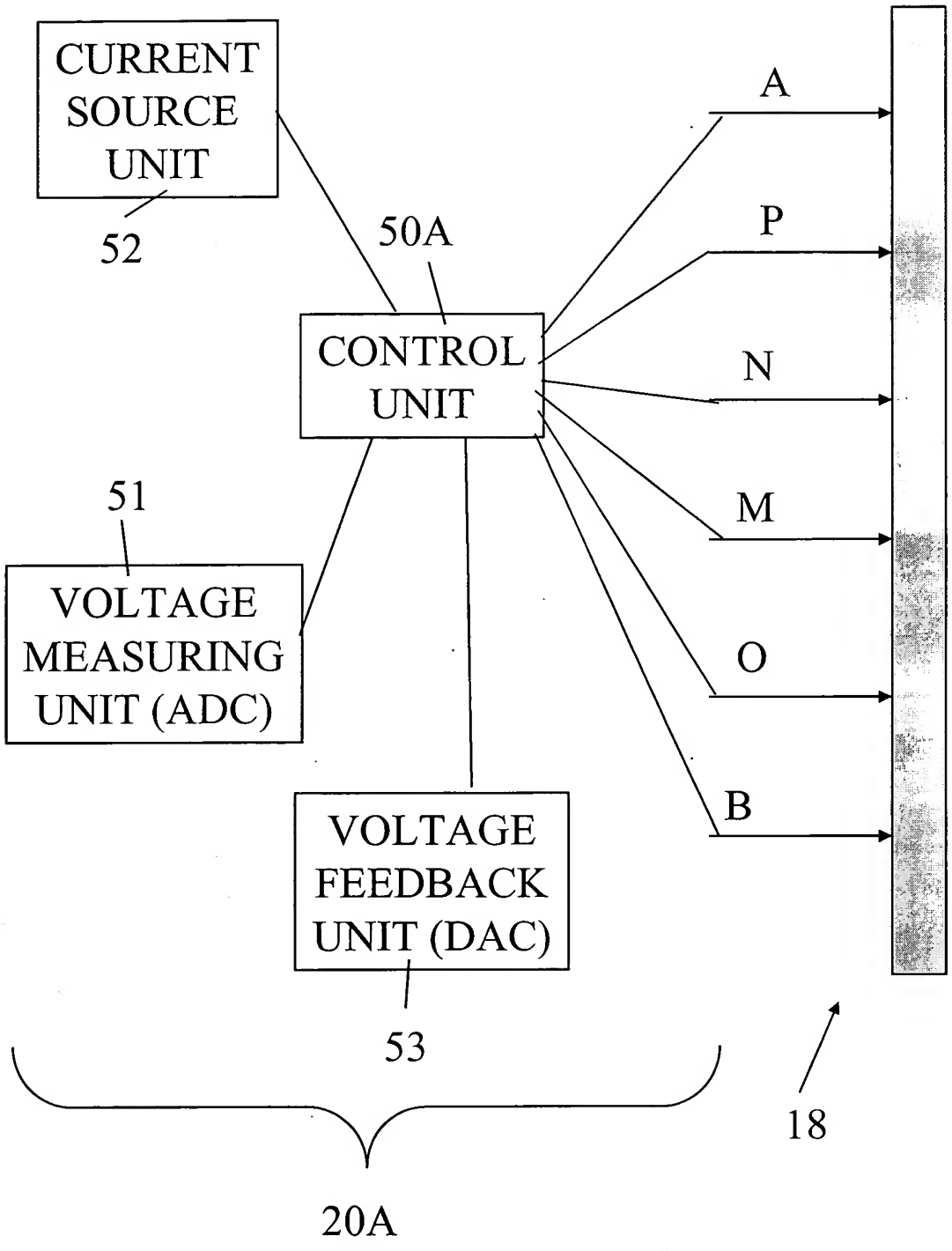
CURRENT SOURCE UNIT
52
50A
CONTROL UNIT
A
P
N
M
O
B
51
VOLTAGE MEASURING UNIT (ADC)
VOLTAGE FEEDBACK UNIT (DAC)
53
18
20A

FIG 5

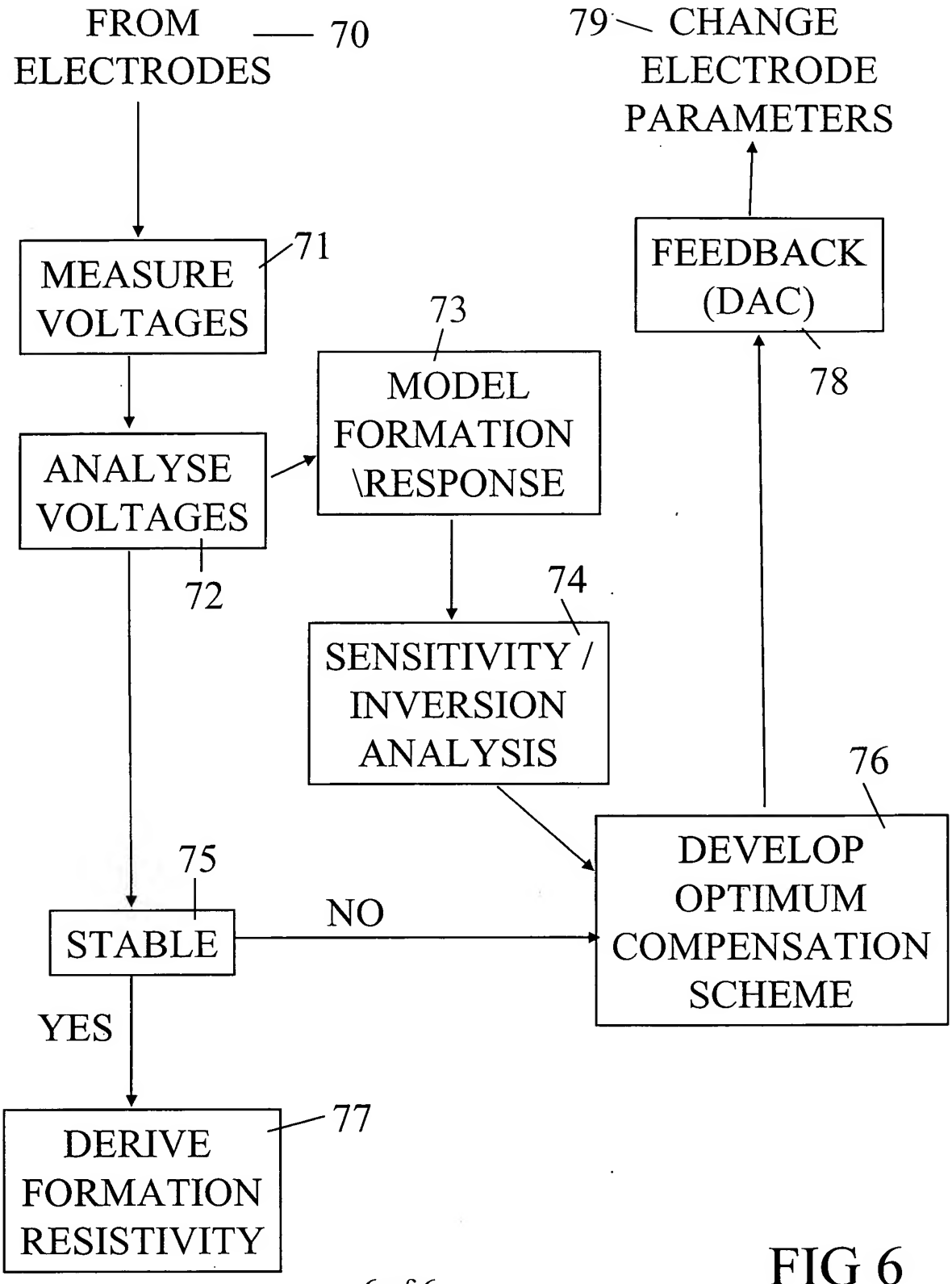
FROM ELECTRODES
70
MEASURE VOLTAGES
71
ANALYSE VOLTAGES
72
MODEL FORMATION \RESPONSE
73
SENSITIVITY / INVERSION ANALYSIS
74
STABLE
75
NO
YES
DERIVE FORMATION RESISTIVITY
77
DEVELOP OPTIMUM COMPENSATION SCHEME
76
FEEDBACK (DAC)
78
79
CHANGE ELECTRODE PARAMETERS

FIG 6